9300 Series PCIe NVMe NAND Flash SSD

MTFDHAL3T2TDR, MTFDHAL3T8TDP, MTFDHAL6T4TDR, MTFDHAL7T6TDP, MTFDHAL12T8TDR, MTFDHAL15T3TDP

Features

- Micron® 3D TLC NAND Flash
- PCI Express Gen3 x4
- NVM Express 1.2
  - Number of namespaces supported: 32
  - Round robin arbitration: Not weighted
  - Interrupt coalescing
  - Number of I/O queue pairs: 128 SQ/CQ
  - Number of admin queue pairs: 1 SQ/CQ
  - 4KB atomic operations
- Capacity (unformatted)[1]
  - 9300 PRO: 3.84TB, 7.68TB, 15.36TB
  - 9300 MAX: 3.2TB, 6.4TB, 12.8TB
- Endurance: Total bytes written (TBW)
  - 3.2TB: Up to 36.2PB
  - 3.84TB: Up to 34.3PB
  - 6.4TB: Up to 72.4PB
  - 7.68TB: Up to 72.0PB
  - 12.8TB: Up to 144.8PB
  - 15.36TB: Up to 137.3PB
- Industry-standard 512 byte and 4096 byte sector size support
- Security
  - Digitally signed firmware
- Surprise insertion/surprise removal (SISR) and hot-plug capable
- Self-monitoring, analysis, and reporting technology (SMART)
- Performance[2]
  - Sequential 128KB READ: Up to 3500 MB/s
  - Sequential 128KB WRITE: Up to 3500 MB/s
  - Random 4KB READ: Up to 850,000 IOPS
  - Random 4KB WRITE: Up to 310,000 IOPS
- Latency[3]
  - READ (TYP): 86µs
  - WRITE (TYP): 11µs
- Reliability
  - MTTF: 2 million device hours[4]
  - Static and dynamic wear leveling
  - Uncorrectable bit error rate (UBER): <1 sector per 10^{17} bits read
  - End-to-end data protection
  - Full power-loss protection
- Non-operating shock: 1000G @ 0.5ms
- Non-operating vibration: $3.1G_{RMS}$ 5–800Hz
- Operating temperature[5]
  - Commercial (0°C to +70°C)
- Field upgradeable firmware
- Operating systems supported natively
  - Microsoft Windows Server® 2016, 2019
  - Ubuntu® 12.04.03+
  - CentOS® 6.5+
  - RHEL® 6.5+
  - SLES®12+
  - VMware® ESXi 5.5+, vSAN 6.0+
  - FreeBSD® 9+
  - UEFI 2.3.1+
  - Intel SPDK
- Operating systems supported by the Micron driver
  - Microsoft Windows Server® 2012R2
- Form factor
  - U.2: 100.45 × 70.10 × 15.00mm
- Electrical specification
  - Power supply: 12V ±8%
  - AUX SMBus supply: 3.3V ±8%

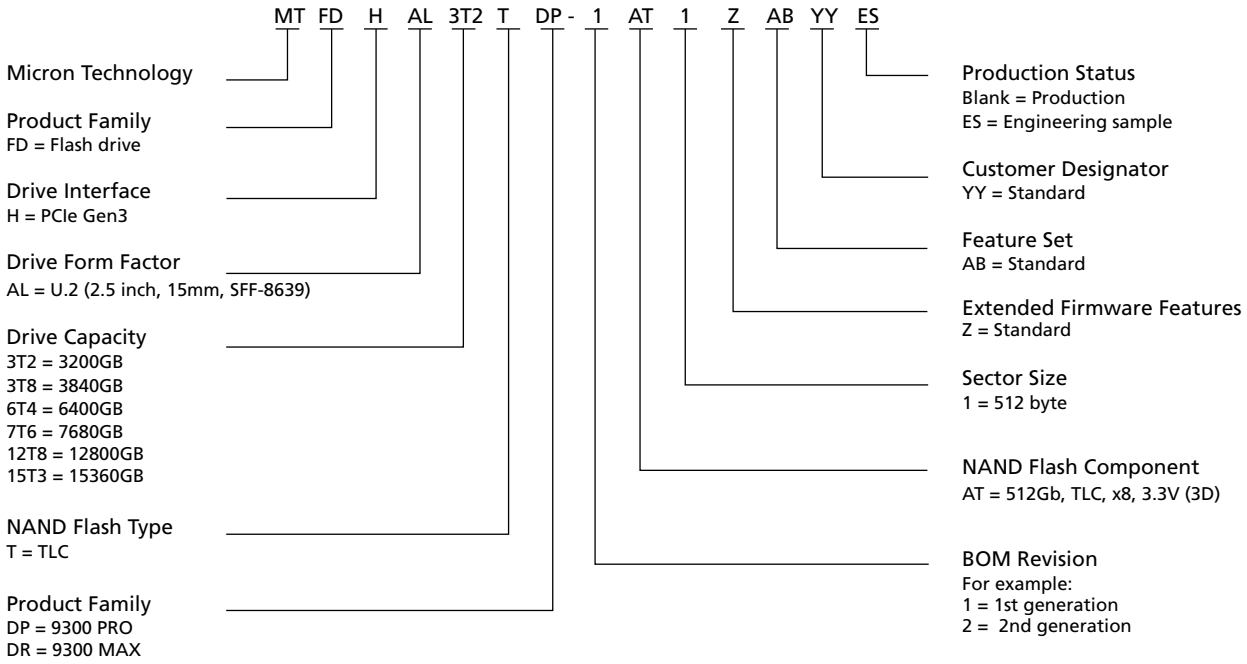
Notes:
1. User capacity: 1TB = 1 trillion bytes.
2. Steady state as defined by SNIA Solid State Storage Performance Test Specification Enterprise v1.1.
3. 4KB, queue depth 1 transfers used for READ/WRITE latency values.
4. The product achieves a mean time to failure (MTTF) based on population statistics not relevant to individual units.
5. Temperature measured by SMART.

Warranty: Contact your Micron sales representative for further information regarding the product, including product warranties.

Part Numbering Information

Micron's SSD devices are available in different configurations and capacities. The chart below is a comprehensive list of options for the 9300 series devices; not all options listed can be combined to define an offered product. Visit www.micron.com for a list of valid part numbers.

Figure 1: Part Number Chart



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General Description

The Micron 9300 NVMe Series SSDs are Micron's flagship performance product line.

These products utilize a Gen3 PCIe interface, the Non-Volatile Memory Express protocol and Micron's own high-speed NAND to provide high throughput and IOPS, very low latency, and consistent quality of service.

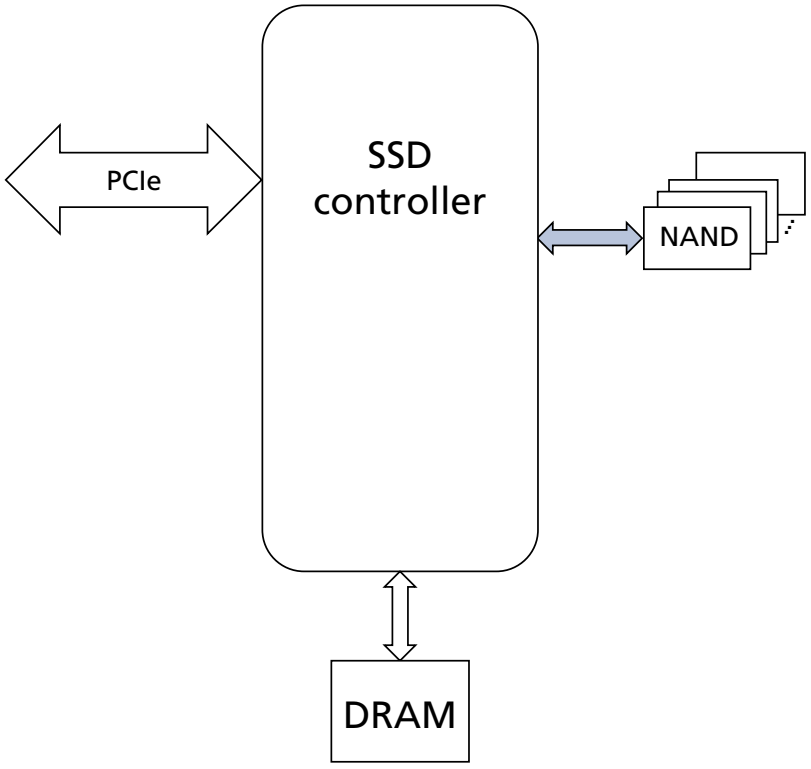
The 9300 product line has Micron's Flex Capacity feature, which enables users to actively tune capacity to optimize drive performance and drive writes per day (DWPD), and is available in high capacities up to 15TBs.

Reliability assurance measures include cyclic redundancy checks (CRC), end-to-end data path protection, capacitor-backed power loss protection and Micron's extensive validation, quality and reliability testing. It features thermal monitoring and protection, SMART attributes for status polling and SMBus for out-of-band management.

The Micron 9300 has two endurance classes: the PRO for read-centric use at roughly 1 DWPD, and the MAX for mixed-use workloads at about 3 DWPD.

The PRO is available in 3.84TB, 7.68TB, and 15.36TB capacities while the MAX is available in 3.2TB, 6.4TB, and 12.8TB capacities.

Figure 2: Functional Block Diagram



Performance

Measured performance can vary for a number of reasons. The major factors affecting drive performance are the capacity of the drive and the interface of the host. Additionally, overall system performance can affect the measured drive performance. When comparing drives, it is recommended that all system variables are the same, and only the drive being tested varies.

Performance numbers will vary depending on the host system configuration.

Table 1: Drive Performance

Parameter	9300 PRO (TB)			9300 MAX (TB)			Unit
	3.84	7.68	15.36	3.2	6.4	12.8	
Sequential read (128KB transfer)	3500	3500	3500	3500	3500	3500	MB/s
Sequential write (128KB transfer)	3100	3500	3500	3100	3500	3500	MB/s
Random read (4KB transfer)	835,000	850,000	850,000	835,000	850,000	850,000	IOPS
Random write (4KB transfer)	105,000	145,000	150,000	210,000	310,000	310,000	IOPS
70/30 Random read write (4KB transfer)	245,000	360,000	325,000	410,000	555,000	460,000	IOPS
READ latency (TYP)	86	86	86	86	86	86	µs
WRITE latency (TYP)	11	11	11	11	11	11	µs
READ latency (99%)	120	120	120	120	120	120	µs
WRITE latency (99%)	30	30	30	30	30	30	µs

Notes:
1. Performance specifications shown are with power limiting off. See the Electrical Characteristics section for more details.
2. Performance is steady state as defined by SNIA Solid State Storage Performance Test Specification Enterprise v1.1.
3. Performance may vary up to 10% over life of drive.
4. 4KB transfers with a queue depth of 1 are used to measure READ/WRITE latency values.
5. System variations and HBA used will affect measured results.

Logical Block Address Configuration

The drive is set to report the number of logical block addresses (LBA) that will ensure sufficient storage space for the specified capacity. Standard LBA settings, based on the IDEMA standard (LBA1-03), are shown below.

Table 2: Standard LBA Settings

Capacity (TB)	512-Byte Sector LBA Count	4096-Byte Sector LBA Count
3.2	6,251,233,968	781,404,246
3.84	7,501,476,528	937,684,566
6.4	12,502,446,768	1,562,805,846
7.68	15,002,931,888	1,875,366,486
12.8	25,004,872,368	3,125,609,046
15.36	30,005,842,608	3,750,730,326

Note: 1. System boot required following a FormatNVM that changes sector size.

Reliability

The SSD incorporates advanced technology for defect and error management, using various combinations of hardware-based error correction algorithms and firmware-based static and dynamic wear-leveling algorithms.

Over the life of the SSD, uncorrectable errors may occur. An uncorrectable error is defined as data that is reported as successfully programmed to the SSD but when it is read out of the SSD, the data differs from what was programmed.

Table 3: Uncorrectable Bit Error Rate

Uncorrectable Bit Error Rate	Operation
<1 sector per 10^{17} bits read	READ

Mean Time to Failure

Mean time to failure (MTTF) for the SSD can be predicted based on the component reliability data using the methods referenced in the Telcordia SR-332 reliability prediction procedures for electronic equipment.

Table 4: MTTF

Capacity	MTTF (Operating Hours)
All capacities	2 million

Note: 1. The product achieves a mean time to failure (MTTF) based on population statistics, not relevant to individual units.

Endurance

SSD endurance is dependent on many factors, including: usage conditions applied to the drive, drive performance and capacity, formatted sector size, error correction codes (ECCs) in use, internal NAND PROGRAM/ERASE cycles, write amplification factor, wear-leveling efficiency of the drive, over-provisioning ratio, valid user data on the drive, drive temperature, NAND process parameters, and data retention time.The device is designed to operate under a wide variety of conditions, while delivering the maximum performance possible and meeting enterprise market demands.

While actual endurance varies depending on conditions, the drive lifetime can be estimated based on capacity, assumed fixed-use models, ECC, and formatted sector size.

Lifetime estimates for the device are shown in the following tables in total bytes written.

Table 5: Total Bytes Written

Model	Capacity (TB)	4K Random Total Bytes Written (PB)	128K Sequential Total Bytes Written (PB)
9300 PRO	3.84	8.4	34.3
	7.68	16.8	72.0
	15.36	33.6	137.3
9300 MAX	3.2	18.6	36.2
	6.4	37.3	72.4
	12.8	74.7	144.8

Notes:
1. All values provided are for reference only and are not warrantied values. For warranty information, visit https://www.micron.com/support/sales-support/returns-and-warranties/enterprise-ssd-warranty or contact your Micron sales representative.
2. Values represent the theoretical maximum endurance for the given transfer size and type. Actual lifetime will vary by workload. Refer to Percentage Used in the SMART/Health Information (Log Identifier 02h) to check the device life used.

Electrical Characteristics

Environmental conditions beyond those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Power Consumption

Parameter	9300 PRO (TB)			9300 MAX (TB)			Unit
	3.84	7.68	15.36	3.2	6.4	12.8	
128K sequential reads (Maximum RMS)	13	13	14	13	13	13	W
128K sequential writes (Maximum RMS)	15	20	21	15	21	21	
128K sequential reads (Average RMS)	14	12	14	12	14	13	
128K sequential writes (Average RMS)	14	18	17	14	17	18	
4K random reads (Average RMS)	13	16	16	13	13	15	
4K random writes (Average RMS)	13	17	17	14	17	17	
Mixed 70/30 read/write (Average RMS)	13	16	15	13	15	14	

Notes:
1. Power limiting is configured through Set/Get Features Power Management.
2. Power consumption measurements are for reference only; actual workload power consumption will vary.

Table 7: Operating Voltage

Power Rail	Electrical Characteristic	Value
12V	Operating voltage	12Vdc (±8%)
	MIN/MAX rise time	10ms/100ms
	Fall time	<5s
	MIN power-off time	15mS
	Inrush current (typical peak)	3.0A
	MAX average current (RMS)	3.0A
$3.3V_{AUX}$	Operating voltage	3.3Vdc (±8%)
	MIN/MAX rise time	1ms/50ms
	MIN/MAX fall time	1ms/5s
	MAX average current	20mA

Table 8: Temperature and Airflow

Temperature and Airflow	Specification	Notes
Operating temperature (as indicated by the SMART temperature attribute)	0°C to 70°C	1
Operating ambient temperature	0°C to 35°C	2
Operating airflow	450 LFM @ 25°C ambient	3
Storage temperature	–40°C to 85°C	
Rate of temperature change	20°C/hr	
Relative humidity (non condensing)	25% to 95%	

Notes:
1. If SMART temperature exceeds 75°C, performance will be throttled.
2. Temperature of air impinging on the drive.
3. Airflow must flow along the length of the drive and is measured upstream.

Table 9: Shock and Vibration

Parameter/Condition	Specification
Non-operating shock	1000G @ 0.5ms half-sine
Non-operating vibration	3.1 G_{RMS} 5–800Hz @ 30 min/axis

Note:
1. Shock and vibration ratings refer to the ability to withstand stress events only. Prolonged or repeated exposure to conditions listed or greater stresses may result in permanent damage to the device. Functional operation of the device under these conditions is not implied. See warranty for more information.

Data Retention

Data retention refers to the capability of the SSD media (that is, NAND flash) to retain programmed data. The three primary factors that affect data retention are:

- Power-on/power-off state: Data retention generally improves when the SSD is in use (that is, not shelved in a power-off state).
- Temperature: Data retention decreases as the temperature increases.
- Number of PROGRAM/ERASE cycles on the media: When the SSD ships from the factory, it is typically able to retain user data for up to 5 years in a powered-off state.

Data retention is guaranteed for three months at 40ºC (MAX), which assumes worst-case power and media wear (the SSD remains in a powered-off state and has reached end of life).

Wear Leveling

The 9300 uses sophisticated wear-leveling algorithms to maximize endurance by distributing PROGRAM/ERASE cycles uniformly across all blocks in the array. Both static and dynamic wear leveling are utilized to optimize the drive's lifespan. Both types of wear leveling aim to distribute "hot" data away from blocks that have experienced relatively heavy wear. Static wear leveling accomplishes this by moving data that has not been modified for an extended period of time out of blocks that have seen few PROGRAM/ERASE cycles and into more heavily worn blocks. This frees up fresher blocks for new data while reducing expected wear on tired blocks. Dynamic wear leveling, by contrast, acts on in-flight data to ensure it is preferentially written to the leastworn free blocks rather than those closer to the end of their rated life. These techniques are used together within the controller to optimally balance the wear profile of the NAND array.

Firmware Update Capability

The 9300 supports firmware updates as defined by the NVMe specification. When a FIRMWARE DOWNLOAD command completes, a FIRMWARE COMMIT command must be issued. Firmware activation is supported without a controller reset.

Power-Loss Subsystem and Rebuild

The 9300 supports an unexpected power loss with a power-backed write cache. No user data is lost during an unexpected power loss. When power is subsequently restored, the SSD returns to a ready state within a maximum of 60 seconds.

Boot

The 9300 supports both legacy boot and UEFI boot.

Dual Port

The 9300 does not support Dual Port configuration.

Identify – Identify Controller Data Structure

Table 10: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
01:00	1344h	**PCI Vendor ID (VID):** Contains the Micron identifier assigned by the PCI SIG.
03:02	1344h	**PCI Subsystem Vendor ID (SSVID):** Contains the Micron identifier assigned by the PCI SIG for the subsystem.
23:04	Variable	**Serial Number (SN):** Contains the serial number for the NVM subsystem as an ASCII string.
63:24	Variable	**Model Number (MN):** Contains the model number for the NVM subsystem as an ASCII string.
71:64	Variable	**Firmware Revision (FR):** Contains the currently active firmware revision for the NVM subsystem.
72	0	**Recommended Arbitration Burst (RAB):** This is the recommended arbitration burst size.
75:73	00A075h	**IEEE OUI Identifier (IEEE):** Contains the organization unique identifier (OUI).
76	0	**Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC):** This field specifies multi-path I/O and namespace sharing capabilities of the controller and NVM subsystem. Bits 7:3 are reserved Bit 2 = 0 the controller is associated with a PCI function Bit 1 = 0 the NVM subsystem contains only a single controller Bit 0 = 0 the NVM subsystem contains only a single PCI Express port
77	5	**Maximum Data Transfer Size (MDTS):** This field indicates the maximum data transfer size between the host and the controller. The host should not submit a command that exceeds this transfer size. If a command is submitted that exceeds the transfer size, then the command is aborted with a status of Invalid Field in command. The value is in units of the minimum memory page size (4096 bytes) and is reported as a power of two (2^n).
79:78	1	**Controller ID (CNTLID):** Contains the NVM subsystem unique controller identifier associated with the controller.
83:80	10200h	**Version (VER):** This register indicates the major and minor version of the NVM Express specification that the controller implementation supports.
87:84	E4E1C0h	**RTD3 Resume Latency (RTD3R):** This field indicates the typical latency in microseconds resuming from Runtime D3 (RTD3).
91:88	989680h	**RTD3 Entry Latency (RTD3E):** This field indicates the typical latency in microseconds to enter Runtime D3 (RTD3).
95:92	100h	**Optional Asynchronous Events Supported (OAES):** This field indicates the optional asynchronous events supported by the controller. A controller shall not send optional asynchronous events before they are enabled by host software. Bits 31:9 are reserved Bit 8 = 1 the controller supports sending the Namespace Attribute Changed event Bits 7:0 are reserved
239:96	–	Reserved.
255:240	0	**NVMe Management Interface:** NVMe Management Interface is not supported.

Table 10: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
257:256	0000000000001110b	**Optional Admin Command Support (OACS):** This field indicates the optional Admin commands supported by the controller. Bits 15:4 are reserved. Bit 3 = 1 the controller supports the NAMESPACE MANAGEMENT and NAMESPACE ATTACHMENT commands Bit 2 = 1 the controller supports the FIRMWARE COMMIT and FIRMWARE IMAGE DOWNLOAD commands Bit 1 = 1 the controller supports the FORMAT NVM command Bit 0 = 0 the controller does not support the SECURITY SEND and SECURITY RECEIVE commands
258	3h	**Abort Command Limit (ACL):** This field is used to convey the maximum number of concurrently outstanding ABORT commands supported by the controller. This is a 0's based value.
259	4h	**Asynchronous Event Request Limit (AERL):** This field is used to convey the maximum number of concurrently outstanding ASYNCHRONOUS EVENT REQUEST commands supported by the controller. This is a 0's based value.
260	00010111b	**Firmware Updates (FRMW):** This field indicates capabilities regarding firmware updates. Bits 7:5 are reserved Bit 4 = 1 the controller supports firmware activation without a reset Bits 3:1 = 011 the number of firmware slots that the controller supports Bit 0 = 1 the first firmware slot (slot 1) is read only
261	00000010b	**Log Page Attributes (LPA):** This field indicates optional attributes for log pages that are accessed via the GET LOG PAGE command. Bits 7:3 are reserved Bit 2 = 0 the controller does not support extended data for the Get log page Bit 1 = 1 the controller supports the Command Effects log page Bit 0 = 0 the controller does not support the SMART/Health Information log page on a per namespace basis
262	62	**Error Log Page Entries (ELPE):** This field indicates the number of Error Information log entries that are stored by the controller. This field is a 0's based value.
263	15	**Number of Power States Support (NPSS):** This field indicates the number of NVM Express power states supported by the controller. This is a 0's based value.
264	1	Reserved.
265	0	**Autonomous Power State Transition Attributes (APSTA):** This field indicates the attributes of the autonomous power state transition feature. Bits 7:1 are reserved Bit 0 = 0 the controller does not support autonomous power state transitions
267:266	15Ch	**Warning Composite Temperature Threshold (WCTEMP):** This field indicates the minimum Composite Temperature field value (Temperature value reported in the SMART/Health Information log) that indicates an overheating condition during which controller operation continues. Immediate remediation is recommended (for example, additional cooling or workload reduction). The platform should strive to maintain a composite temperature below this value.

Table 10: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
269:268	161h	**Critical Composite Temperature Threshold (CCTEMP):** This field indicates the minimum Composite Temperature field value (Temperature value reported in the SMART/Health Information log) that indicates a critical overheating condition (for example, automatic device shutdown).
271:270	1200	**Maximum Time for Firmware Activation (MTFA):** This field indicates the maximum time the controller temporarily stops processing commands to activate the firmware image. This field is specified in 100 millisecond units.
275:272	0	**Host Memory Buffer Preferred Size (HMPRE):** Host Memory Buffer Preferred Size is not supported.
279:276	0	**Host Memory Buffer Minimum Size (HMMIN):** Host Memory Buffer Minimum Size is not supported.
295:280	Variable	**Total NVM Capacity (TNVMCAP):** This field indicates the total NVM capacity in the NVM subsystem. The value is in bytes.
311:296	Variable	**Unallocated NVM Capacity (UNVMCAP):** This field indicates the unallocated NVM capacity in the NVM subsystem. The value is in bytes.
315:312	0	**Replay Protected Memory Block Support (RPMBS):** Replay Protected Memory Blocks is not supported.
511:316	–	Reserved.
512	66h	**Submission Queue Entry Size (SQES):** This field defines the required and maximum submission queue entry size when using the NVM command set. Bits 7:4 = 6 defines the maximum submission queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n) Bits 3:0 = 6 defines the required submission queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n)
513	44h	**Completion Queue Entry Size (CQES):** This field defines the required and maximum completion queue entry size when using the NVM command set. Bits 7:4 = 4 defines the maximum completion queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n) Bits 3:0 = 4 defines the required completion queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n)
515:514	–	Reserved.
519:516	32	**Number of Namespaces (NN):** This field defines the number of valid namespaces present for the controller.
521:520	0000000000010100b	**Optional NVM Command Support (ONCS):** This field indicates the optional NVM commands and features supported by the controller. Bits 15:6 are reserved Bit 5 = 0 the controller does not support reservations Bit 4 = 1 the controller supports the save field in the SET FEATURES command and the select field in the GET FEATURES command Bit 3 = 0 the controller does not support the WRITE ZEROS command Bit 2 = 1 the controller supports the DATASET MANAGEMENT command Bit 1 = 0 the controller does not support the WRITE UNCORRECTABLE command Bit 0 = 0 the controller does not support the COMPARE command
523:522	0	**Fused Operation Support (FUSES):** Fused Operation is not supported.

Table 10: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
524	00000100b	**Format NVM Attributes (FNA):** This field indicates attributes for the FORMAT NVM command. Bits 7:3 are reserved Bit 2 = 1 indicates cryptographic erase is supported as part of the secure erase functionality. Cryptographic erase will perform a TRIM of all LBAs on namespaces formatted as 512-byte sector size. Cryptographic erase will perform a TRIM of all LBAs and delete the namespace encryption key on namespaces formatted as 4096-byte sector size. Bit 1 = 0 cryptographic erase or user data erase as part of a format are performed on a per namespace basis Bit 0 = 0 the controller supports format on a per namespace basis
525	0	**Volatile Write Cache (VWC):** This field indicates attributes related to the presence of a volatile write cache in the implementation. Bits 7:1 are reserved Bit 0 = 0 volatile write cache is not present. FLUSH commands complete successfully and have no effect, SET FEATURES with the volatile write cache identifier field set shall fail with Invalid Field status, and GET FEATURES with the volatile write cache identifier field set shall fail with Invalid Field status.
527:526	0	**Atomic Write Unit Normal (AWUN):** This field indicates the size of the WRITE operation guaranteed to be written atomically to the NVM across all namespaces with any supported namespace format during normal operation. This field is specified in logical blocks and is a 0's based value. If a specific namespace guarantees a larger size than is reported in this field, then this namespace specific size is reported in the NAWUN field in the Identify Namespace data structure. If a write command is submitted with size less than or equal to the AWUN value, the host is guaranteed that the WRITE command is atomic to the NVM with respect to other READ or WRTE commands. If a WRITE command is submitted with size greater than the AWUN value, then there is no guarantee of command atomicity. AWUN does not have any applicability to write errors caused by power failure (refer to Atomic Write Unit Power Fail).
529:528	0	**Atomic Write Unit Power Fail (AWUPF):** This field indicates the size of the write operation guaranteed to be written atomically to the NVM across all namespaces with any supported namespace format during a power fail or error condition. If a specific namespace guarantees a larger size than is reported in this field, then this namespace specific size is reported in the NAWUPF field in the Identify Namespace data structure. This field is specified in logical blocks and is a 0's based value. The AWUPF value shall be less than or equal to the AWUN value. If a WRITE command is submitted with size less than or equal to the AWUPF value, the host is guaranteed that the write is atomic to the NVM with respect to other WRITE or WRITE commands. If a WRITE command is submitted that is greater than this size, there is no guarantee of command atomicity. If the write size is less than or equal to the AWUPF value and the WRITE command fails, then subsequent READ commands for the associated logical blocks shall return data from the previous successful WRITE command. If a WRITE command is submitted with size greater than the AWUPF value, then there is no guarantee of data returned on subsequent reads of the associated logical blocks.
530	1	Reserved.

Table 10: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
531	–	Reserved.
533:532	0	**Atomic Compare & Write Unit (ACWU):** Atomic Compare & Write Unit is not supported.
535:534	–	Reserved.
539:536	0	**SGL Support (SGLS):** SGL is not supported.
2047:540	–	Reserved.
2079:2048	0000000000000000000000000000000000000000000000000000064000000640000009C4h	**Power State 0 Descriptor (PSD0):** This field indicates the characteristics of power state 0. The format of this field is defined in Table 11.
2111:2080	0000000000000000000000000000000000000001010101000000730000007300000960h	**Power State 1 Descriptor (PSD1):** This field indicates the characteristics of power state 1. The format of this field is defined in Table 11.
2143:2112	0000000000000000000000000000000000000002020202000000820000008200008FCh	**Power State 2 Descriptor (PSD2):** This field indicates the characteristics of power state 2. The format of this field is defined in Table 11.
2175:2144	0000000000000000000000000000000000000003030303000000910000009100000898h	**Power State 3 Descriptor (PSD3):** This field indicates the characteristics of power state 3. The format of this field is defined in Table 11.
2207:2176	0000000000000000000000000000000000000004040404000000A0000000A000000834h	**Power State 4 Descriptor (PSD4):** This field indicates the characteristics of power state 4. The format of this field is defined in Table 11.
2239:2208	0000000000000000000000000000000000000005050505000000AF000000AF000007D0h	**Power State 5 Descriptor (PSD5):** This field indicates the characteristics of power state 5. The format of this field is defined in Table 11.
2271:2240	0000000000000000000000000000000000000006060606000000BE000000BE0000076Ch	**Power State 6 Descriptor (PSD6):** This field indicates the characteristics of power state 6. The format of this field is defined in Table 11.
2303:2272	0000000000000000000000000000000000000007070707000000CD000000CD000008708h	**Power State 7 Descriptor (PSD7):** This field indicates the characteristics of power state 7. The format of this field is defined in Table 11.
2335:2304	0000000000000000000000000000000000000008080808000000DC000000DC000006A4h	**Power State 8 Descriptor (PSD8):** This field indicates the characteristics of power state 8. The format of this field is defined in Table 11.

Table 10: Identify – Identify Controller Data Structure (Continued)

Bytes	Default Value	Description
2367:2336	0000000000000000000000000000000000000009090909000000EB000000EB00000640h	**Power State 9 Descriptor (PSD9):** This field indicates the characteristics of power state 9. The format of this field is defined in Table 11.
2399:2368	0000000000000000000000000000000000000A0A0A0A000000FA000000FA000005DCh	**Power State 10 Descriptor (PSD10):** This field indicates the characteristics of power state 10. The format of this field is defined in Table 11.
2431:2400	0000000000000000000000000000000000000B0B0B0B0000010900000109000005 78h	**Power State 11 Descriptor (PSD11):** This field indicates the characteristics of power state 11. The format of this field is defined in Table 11.
2463:2432	0000000000000000000000000000000000000C0C0C0C0000011800000118000005 14h	**Power State 12 Descriptor (PSD12):** This field indicates the characteristics of power state 12. The format of this field is defined in Table 11.
2495:2464	0000000000000000000000000000000000000D0D0D0D0000012700000127000004B0h	**Power State 13 Descriptor (PSD13):** This field indicates the characteristics of power state 13. The format of this field is defined in Table 11.
2527:2496	0000000000000000000000000000000000000E0E0E0E0000013600000136000004 4Ch	**Power State 14 Descriptor (PSD14):** This field indicates the characteristics of power state 14. The format of this field is defined in Table 11.
2559:2528	0000000000000000000000000000000000000F0F0F0F0000014500000145000003E8h	**Power State 15 Descriptor (PSD15):** This field indicates the characteristics of power state 15. The format of this field is defined in Table 11.
4095:2560	–	Reserved.

Table 11: Power State Descriptor Data Structure

Bits	Description
15:0	**Maximum Power (MP):** This field indicates the maximum power consumed by the NVM subsystem in this power state. The power in Watts is equal to the value in this field multiplied by the scale specified in the Maximum Power Scale field.
23:16	Reserved.
24	**Max Power Scale (MPS):** This field indicates the scale for the Maximum Power field in 0.01 Watts.
25	**Non-Operational State (NOPS):** This field indicates whether the controller processes I/O commands in this power state. If this field is cleared to 0, then the controller processes I/O commands in this power state. If this field is set to 1, then the controller does not process I/O commands in this power state.
31:26	Reserved.
63:32	**Entry Latency (ENLAT):** This field indicates the maximum entry latency in microseconds associated with entering this power state.

Table 11: Power State Descriptor Data Structure (Continued)

Bits	Description
95:64	**Exit Latency (EXLAT):** This field indicates the maximum exit latency in microseconds associated with exiting this power state.
100:96	**Relative Read Throughput (RRT):** This field indicates the relative read throughput associated with this power state. A lower value means higher read throughput.
103:101	Reserved.
108:104	**Relative Read Latency (RRL):** This field indicates the relative READ latency associated with this power state. A lower value means lower READ latency.
111:109	Reserved.
116:112	**Relative Write Throughput (RWT):** This field indicates the relative write throughput associated with this power state. A lower value means higher write throughput.
119:117	Reserved.
124:120	**Relative Write Latency (RWL):** This field indicates the relative WRITE latency associated with this power state. A lower value means lower WRITE latency.
127:125	Reserved.
143:128	**Idle Power (IDLP):** This field indicates the typical power consumed by the NVM subsystem over 30 seconds in this power state when idle. The measurement starts after the NVM subsystem has been idle for 10 seconds. The power in Watts is equal to the value in this field multiplied by the scale indicated in the Idle Power Scale field.
149:144	Reserved.
151:150	**Idle Power Scale (IPS):** This field indicates the scale for the Idle Power field.
159:152	Reserved.
175:160	**Active Power (ACTP):** This field indicates the largest average power consumed by the NVM subsystem over a 10 second period in this power state with the workload indicated in the Active Power Workload field. The power in Watts is equal to the value in this field multiplied by the scale indicated in the Active Power Scale field.
178:176	**Active Power Workload (APW):** This field indicates the workload used to calculate maximum power for this power state.
181:179	Reserved.
183:182	**Active Power Scale (APS):** This field indicates the scale for the Active Power field.
255:184	Reserved.

Table 12: Identify — Identify Namespace Data Structure

Bits	Default Value	Description
07:00	Variable	**Namespace Size (NSZE):** This field indicates the total size of the namespace in logical blocks. A namespace of size n consists of LBA 0 through (n - 1). The number of logical blocks is based on the formatted LBA size.
15:08	Variable	**Namespace Capacity (NCAP):** This field indicates the maximum number of logical blocks that may be allocated in the namespace at any point in time. The number of logical blocks is based on the formatted LBA size. A logical block is allocated when it is written with a WRITE or WRITE UNCORRECTABLE command. A logical block may be deallocated using the DATA-SET MANAGEMENT command.
23:16	Variable	**Namespace Utilization (NUSE):** This field indicates the current number of logical blocks allocated in the namespace. This field is equal to the Namespace Capacity. The number of logical blocks is based on the formatted LBA size. When using the NVM command set: A logical block is allocated when it is written with a WRITE or WRITE UNCORRECTABLE command. A logical block may be deallocated using the DATASET MANAGEMENT command.
24	8	**Namespace Features (NSFEAT):** This field defines features of the namespace. Bits 7:4 are reserved Bit 3 = 1 the non-zero NGUID and non-zero EUI64 fields for this namespace are never reused by the controller. Bit 2 = 0 the controller does not support the Deallocated or Unwritten Logical Block error Bit 1 = 0 the controller does not support the fields NAWUN, NAWUPF, and NACWU for the namespace Bit 0 = 0 thin provisioning is not supported, the Namespace Size and Namespace Capacity fields report the same value
25	3	**Number of LBA Formats (NLBAF):** This field defines the number of supported LBA data sizes supported by the namespace. This is a 0's based value.
26	0	**Formatted LBA Size (FLBAS):** This field indicates the LBA data size that the namespace has been formatted with. Bits 7:5 are reserved Bit 4 = 0 the controller does not support metadata Bits 3:0 = 0 indicates a single supported LBA format.
27	0	**Metadata Capabilities (MC):** Metadata Capabilities is not supported.
28	0	**End-to-end Data Protection Capabilities (DPC):** End-to-end Data Protection Capabilities is not supported.
29	0	**End-to-end Data Protection Type Settings (DPS):** End-to-end Data Protection Type Settings is not supported.
30	1	**Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC):** This field specifies multi-path I/O and namespace sharing capabilities of the namespace. Bits 7:1 are reserved. Bit 0 = 1 the namespace is a shared namespace.
31	0	**Reservation Capabilities (RESCAP):** Reservation Capabilities are not supported.
32	0	**Format Progress Indicator (FPI):**Format Progress Indicator field is not supported.
33	–	Reserved.
35:34	0	**Namespace Atomic Write Unit Normal (NAWUN):** Namespace Atomic Write Unit Normal is not supported.

Table 12: Identify — Identify Namespace Data Structure (Continued)

Bits	Default Value	Description
37:36	0	**Namespace Atomic Write Unit Power Fail (NAWUPF):** Namespace Atomic Write Unit Power Fail is not supported.
39:38	0	**Namespace Atomic Compare & Write Unit (NACWU):** Namespace Atomic Compare & Write Unit is not supported.
41:40	0	**Namespace Atomic Boundary Size Normal (NABSN):** Namespace Atomic Boundary Size Normal is not supported.
43:42	0	**Namespace Atomic Boundary Offset (NABO):** Namespace Atomic Boundary Offset is not supported.
45:44	0	**Namespace Atomic Boundary Size Power Fail (NABSPF):** Namespace Atomic Boundary Size Power Fail is not supported.
47:46	–	Reserved.
63:48	Variable	**NVM Capacity (NVMCAP):** This field indicates the total size of the NVM allocated to this namespace. The value is in bytes.
103:64	–	Reserved.
119:104	Variable	**Namespace Globally Unique Identifier (NGUID):** This field contains the 128-bit Name-space Globally Unique Identifier value.
127:120	Variable	**IEEE Extended Unique Identifier (EUI64):** This field contains the 64-bit IEEE Extended Unique Identifier value.
131:128	00090000h	**LBA Format 0 Support (LBAF0):** This field indicates the LBA format 0 that is supported by the controller. Bits 31:26 are reserved. Bits 25:24 = 0 relative performance of the LBA format is not supported. Bits 23:16 = 09 indicates the LBA data size supported, the value is reported in terms of a power of two (2^n) = 512 byte LBA data size. Bits 15:0 = 0 metadata is not supported.
135:132	000C0000h	**LBA Format 1 Support (LBAF1):** This field indicates the LBA format 1 that is supported by the controller. Bits 31:26 are reserved. Bits 25:24 = 0 relative performance of the LBA format is not supported. Bits 23:16 = 0C indicates the LBA data size supported, the value is reported in terms of a power of two (2^n) = 4096 byte LBA data size. Bits 15:0 = 0 metadata is not supported.
139:136	00090000h	**LBA Format 2 Support (LBAF2):** This field indicates the LBA format 2 that is supported by the controller. Bits 31:26 are reserved. Bits 25:24 = 0 relative performance of the LBA format is not supported. Bits 23:16 = 09 indicates the LBA data size supported, the value is reported in terms of a power of two (2^n) = 512 byte LBA data size. Bits 15:0 = 0 metadata is not supported.

Table 12: Identify — Identify Namespace Data Structure (Continued)

Bits	Default Value	Description
143:140	000C0000h	**LBA Format 3 Support (LBAF3):** This field indicates the LBA format 3 that is supported by the controller. Bits 31:26 are reserved. Bits 25:24 = 0 relative performance of the LBA format is not supported. Bits 23:16 = 0C indicates the LBA data size supported, the value is reported in terms of a power of two (2^n) = 4096 byte LBA data size. Bits 15:0 = 0 metadata is not supported.
4095:144	–	Reserved.

Commands

Table 13: Op Codes for Admin Commands

Codes not listed are reserved. All commands in the table are supported.

Command Name	Op Code (hex)
DELETE I/O SUBMISSION QUEUE	00h
CREATE I/O SUBMISSION QUEUE	01h
GET LOG PAGE	02h
DELETE I/O COMPLETION QUEUE	04h
CREATE I/O COMPLETION QUEUE	05h
IDENTIFY	06h
ABORT	08h
SET FEATURES - SET ARBITRATION	09h - 01h
SET FEATURES - SET POWER MANAGEMENT	09h - 02h
SET FEATURES - SET TEMPERATURE THRESHOLD	09h - 04h
SET FEATURES - SET ERROR RECOVERY	09h - 05h
SET FEATURES - SET NUMBER OF QUEUES	09h - 07h
SET FEATURES - SET INTERRUPT COALESCE	09h - 08h
SET FEATURES - SET INTERRUPT VECTOR CONFIGURATION	09h - 09h
SET FEATURES - SET WRITE ATOMICITY	09h - 0Ah
SET FEATURES - SET ASYNC EVENT CONFIGURATION	09h - 0Bh
SET FEATURES - RESERVATION NOTIFICATION MASK	09h - 82h
SET FEATURES – RESERVATION PERSISTENCE	09h – 83h
GET FEATURES - GET ARBITRATION	0Ah - 01h
GET FEATURES - GET POWER MANAGEMENT	0Ah - 02h
GET FEATURES - GET TEMPERATURE THRESHOLD	0Ah - 04h
GET FEATURES - GET ERROR RECOVERY	0Ah - 05h
GET FEATURES - GET NUMBER OF QUEUES	0Ah - 07h
GET FEATURES - GET INTERRUPT COALESCE	0Ah - 08h
GET FEATURES - GET INTERRUPT VECTOR CONFIGURATION	0Ah - 09h
GET FEATURES - GET WRITE ATOMICITY	0Ah - 0Ah
GET FEATURES - GET ASYNC EVENT CONFIGURATION	0Ah - 0Bh
GET FEATURES - RESERVATION NOTIFICATION MASK	0Ah - 82h
GET FEATURES - RESERVATION PERSISTENCE	0Ah - 83h
ASYNCHRONOUS EVENT REQUEST	0Ch
NAMESPACE MANAGEMENT	0Dh
FIRMWARE COMMIT	10h
FIRMWARE IMAGE DOWNLOAD	11h
NAMESPACE ATTACHMENT	15h
FORMAT NVM	80h

Table 14: Op Codes for NVMe Commands

Codes not listed are reserved. All commands in the table are supported.

Command Name	Op Code (hex)
FLUSH	00h
WRITE	01h
READ	02h
DATASET MANAGEMENT – DEALLOCATE (AD)	09h
RESERVATION REGISTER	0Dh
RESERVATION REPORT	0Eh
RESERVATION ACQUIRE	11h
RESERVATION RELEASE	15h

Log Pages

The SSD supports log information as defined in the NVMe specification. Supported information is shown in the following tables:

- Error Information (Log Identifier 01h)
- SMART/Health Information (Log Identifier 02h)
- Firwmare Slot Information (Log Identifier 03h)
- Commands Supported and Effects (Log Identifier 05h)
- Reservation Notification (Log Identifier 80h)
- Micron Vendor Unique SMART (Log Identifier CAh)

Table 15: Error Information (Log Identifier 01h)

Bytes	Name	Description
7:0	Error count	This is a 64-bit incrementing error count, indicating a unique identifier for this error. The error count starts at 1h, is incremented for each unique error log entry, and is retained across power off conditions. A value of 0h indicates an invalid entry; this value may be used when there are lost entries or when there are fewer errors than the maximum number of entries the controller supports.
9:8	Submission queue ID	This field indicates the submission queue Identifier of the command that the error information is associated with. If the error is not specific to a particular command then this field shall be set to FFFFh.
11:10	Command ID	This field indicates the command Identifier of the command that the error is associated with. If the error is not specific to a particular command then this field shall be set to FFFFh.
13:12	Status field	This field indicates the status field for the command that completed. The status field is located in bits 15:01, bit 00 corresponds to the phase tag posted for the command. If the error is not specific to a particular command then this field reports the most applicable status value.
15:14	Parameter error location	This field indicates the byte and bit of the command parameter that the error is associated with, if applicable. If the parameter spans multiple bytes or bits, then the location indicates the first byte and bit of the parameter. Bit 7:0; Byte in command that contained the error. Valid values are 0 to 63. Bit 10:8; Bit in command that contained the error. Valid values are 0 to 7. Bit 15:11; Reserved If the error is not specific to a particular command then this field shall be set to FFFFh.
23:16	LBA	This field indicates the first LBA that experienced the error condition, if applicable.
27:24	Namespace	This field indicates the namespace that the error is associated with, if applicable.
31:28	Reserved	Reserved.
39:32	Command specific information	This field contains command specific information. If used, the command definition specifies the information returned.
63:40	Reserved	Reserved.

Table 16: SMART/Health Information (Log Identifier 02h)

Bytes	Name	Description
0	Critical warning	Indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; multiple bits may be set. If a bit is cleared to 0, the critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. Bit 0; If set to 1, the available spare space has fallen below the threshold. Bit 1; If set to 1, the temperature has exceeded a critical threshold. Bit 2; If set to 1, the device reliability has been degraded due to significant media-related errors or any internal error that degrades device reliability. Bit 3; If set to 1, the media has been placed in read-only mode. Bits 7:4; Reserved
2:1	Temperature	Contains the temperature of the overall device (controller and NVM included) in units of Kelvin. If it exceeds the temperature threshold, an asynchronous event may be issued to the host.
3	Available spare	Contains a normalized percentage (0-100%) of the remaining available spare capacity.
4	Available spare threshold	When the available spare falls below the threshold indicated in this field, an asynchronous event may be issued to the host. The value is indicated as a normalized percentage (0-100%).
5	Percentage used	Contains an estimate of the percentage of the device life used based on the actual device usage and prediction of device life. A value of 100 indicates that the estimated endurance of the device has been consumed, but may not indicate a device failure. The value is allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value shall be updated once per power-on hour (when the controller is not in a sleep state).
31:6	Reserved	Reserved.
47:32	Data units read	Contains the number of 512 byte data units the host has read from the controller; this value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes read) and is rounded up. For the NVM command set, logical blocks read as part of COMPARE and READ operations shall be included in this value.
63:48	Data units written	Contains the number of 512 byte data units the host has written to the controller; this value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes written) and is rounded up. For the NVM command set, logical blocks written as part of WRITE operations shall be included in this value.
79:64	Host READ commands	Contains the number of READ commands completed by the controller. For the NVM command set, this is the number of COMPARE and READ commands.
95:80	Host WRITE commands	Contains the number of WRITE commands completed by the controller. For the NVM command set, this is the number of WRITE commands.
111:96	Controller busy time	Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O queue (specifically, a command was issued via an I/O submission queue tail doorbell write and the corresponding completion queue entry has not been posted yet to the associated I/O completion queue. This value is reported in minutes.
127:112	Power cycles	Contains the number of power cycles.

Table 16: SMART/Health Information (Log Identifier 02h) (Continued)

Bytes	Name	Description
143:128	Power on hours	Contains the number of power-on hours. This does not include time that the controller was powered and in a low-power state condition.
159:144	Unsafe shutdowns	Contains the number of unsafe shutdowns. This count is incremented when a shutdown notification (CC.SHN) is not received prior to loss of power.
175:160	Media and data integrity errors	Contains the number of occurrences where the controller detected an unrecovered data integrity error.
191:176	Number of error info log entries	Contains the number of error information log entries over the life of the controller.
195:192	Warning composite temperature time	Contains the amount of time in minutes that the controller is operational and the composite temperature is greater than or equal to the warning composite temperature threshold (WCTEMP) field and less than the critical composite temperature threshold (CCTEMP) field in the Identify controller data structure.
199:196	Critical composite temperature time	Contains the amount of time in minutes that the controller is operational and the composite temperature is greater the critical composite temperature threshold (CCTEMP) field in the Identify controller data structure.
201:200	Temperature Sensor 1	Contains the current temperature reported by temperature sensor 1.
203:202	Temperature Sensor 2	Contains the current temperature reported by temperature sensor 2.
205:204	Temperature Sensor 3	Contains the current temperature reported by temperature sensor 3.
207:206	Temperature Sensor 4	Contains the current temperature reported by temperature sensor 4.
511:208	Reserved	Reserved.

Table 17: Firmware Slot Information (Log Identifier 03h)

Bytes	Name	Description
0	Active Firmware Info (AFI)	Specifies information about the active firmware revision. Bit 7 is reserved Bits 6:4 indicates the firmware slot that is going to be activated at the next controller reset. Bit 3 is reserved Bits 2:0 indicates the firmware slot from which the actively running firmware revision was loaded.
7:1	Reserved	Reserved.
15:8	Firmware Revision for Slot 1 (FRS1)	Contains the revision of the firmware downloaded to firmware slot 1. Firmware slot is read-only.
23:16	Firmware Revision for Slot 2 (FRS2)	Contains the revision of the firmware downloaded to firmware slot 2.
31:24	Firmware Revision for Slot 3 (FRS3)	Contains the revision of the firmware downloaded to firmware slot 3.
511:32	Reserved	Reserved.

Table 18: Commands Supported and Effects (Log Identifier 05h)

Bytes	Name	Description
3:0	Admin Command Supported 0 (ACS0)	Contains the Command Effect data structure for the Admin command with an opcode value of 0h. The format of this field is defined by the NVM Express specification.
…	…	…
1023:1020	Admin Command Supported 255 (ACS255)	Contains the Command Effect data structure for the Admin command with an opcode value of 255. The format of this field is defined by the NVM Express specification.
1027:1024	I/O Command Supported 0 (IOCS0)	Contains the Command Effect data structure for the I/O command with an opcode value of 0h. The format of this field is defined by the NVM Express specification.
…	…	…
2047:2044	I/O Command Supported 255 (IOCS255)	Contains the Command Effect data structure for the I/O command with an opcode value of 255. The format of this field is defined by the NVM Express specification.
4095:2048	Reserved	Reserved.

Table 19: Reservation Notification (Log Identifier 80h)

Bytes	Name	Description
7:0	Log Page Count	This is a 64-bit incrementing reservation motification log page count, indicating a unique identifier for this notification. The count starts at 0h following a controller reset, is incremented with each unique log entry, and rolls over to zero when the maximum count is reached and a log page is created. A value of 0h indicates an empty log entry.
8	Reservation Notification Log Page Type	This field indicates the Reservation Notification type described by this log page. 0 = Empty log page. GET LOG PAGE command was processed when no unread reservation notification log pages were available. All the fields of an empty log page shall have a value of zero. 1 = Registration preempted. 2 = Reservation released. 3 = Reservation preempted. 255:4 = Reserved.
9	Number of Available Log Pages	This field indicates the number of additional available reservation notification log pages (i.e., the number of unread log pages, not counting this one). If there are more than 255 additional available log pages, then a value of 255 is returned. A value of zero indicates that there are no additional available log pages.
11:10	Reserved	Reserved.
15:12	Namespace ID	This field indicates the namespace ID of the namespace associated with the reservation notification described by this log page.
63:16	Reserved	Reserved.

Table 20: Micron Vendor Unique SMART (Log Identifier CAh)

Bytes	Name	Description
0	F9h	**Total NAND writes:** Reports the cumulative number of writes to NAND in 1GB increments.
4:1	Reserved	
11:5	Total NAND writes	
12	FAh	**Total NAND reads**: Reports the cumulative number of reads from NAND in 1GB increments.
16:13	Reserved	
23:17	Total NAND reads	
24	EAh	**Thermal throttle status and time:** Reports the current throttle status and total throttling time. Byte 29 = If set to 1, throttling is active; if set to 0, throttling is not active Bytes 34:30 = Total throttling time in minutes since power on
28:25	Reserved	
34:29	Thermal throttle status and time	
35	Reserved	
36	E7h	**Lifetime temperature:** Reports the maximum and minimum temperature in degrees Kelvin over the lifetime of the drive. Bytes 42:41 = maximum temperature Bytes 44:43 = minimum temperature Bytes 46:45 = current temperature
40:37	Reserved	
46:41	Lifetime temperature	
47	Reserved	
48	E8h	**Power consumption:** Reports the maximum, minimum, and average power consumption in watts. Bytes 54:53 = maximum power consumption Bytes 56:55 = minimum power consumption Bytes 58:57 = average power consumption
52:49	Reserved	
58:53	Power consumption	
59	Reserved	
60	AFh	**Power on temperature:** Reports the maximum and minimum temperature in degrees Kelvin since the last power on. Bytes 66:65 = maximum temperature Bytes 68:67 = minimum temperature Bytes 70:69 = current temperature
64:61	Reserved	
70:65	Power on temperature	
71	Reserved	

SMBus Out-of-Band Management

SMBus Sideband Management

The 9300 uses the SMBus interface for presenting product data, monitoring drive health, checking drive status before power-up, and error posting.

Protocol supported: Enterprise SSD form factor interface with its accompanying vital product data (VPD) definition.

Management data and vital product data may be accessed at fixed addresses with +3.3V_{AUX} prior to powering up the drive completely. This data continues to be available at this fixed address when the drive is fully powered up.

Table 21: Out-of-Band Management Details

Out-of-Band Specification	SMBUS Address	Alternate Address (due to bit shift)	Out-of-Band Data Structure
Enterprise SSD Form Factor	0x53	0xA6	Vital product data (VPD)
NVMe Management Interface	0x6A	0xD4	Subsystem management data (SMD)

Notes:
1. SMBUS addresses will appear at an alternate address in certain tools due the inclusion of direction bit in the SMBUS spec.
2. Out-of-band management is enabled by default.

Table 22: Vital Product Data (VPD) Structure

Address	#Bytes	Function	Value	Byte Offset	Description
0x53 (7-bit)	3	Class code	02h	0	Device type and programming interface
			08h	1	
			01h	2	
	2	ID	44h	3	PCI-SIG vendor ID
			13h	4	
	20		Variable	5–24	Serial number
	40		Variable	25–64	Model number
	1	PCIe port0 capabilities	03h	65	Maximum link speed
	1		04h	66	Maximum link width
	1	PCIe port1 capabilities	03h	67	Maximum link speed
	1		02h	68	Maximum link width
	1	Initial power requirements	08h	69	12V power rail initial power requirement (W)
	2	Reserved	0	70–71	Reserved
	1	Maximum power requirements	24h	72	12V power rail maximum power requirement (W)
	2	Reserved	0	73–74	Reserved
	2	Capability list pointer	4Dh	75	16b address offset pointers to start of capability list; see Capability List Pointer table
			00h	76	

Table 23: Capability List Pointer

Address	#Bytes	Value	Byte Offset	R/W	Description
0x004D	2	A5h	0	RO	PCI-SIG vendor-specific capability
		00h	1		
	2	00h	2	RO	Pointer to next capability
		00h	3		
	2	44h	4	RO	PCI-SIG vendor ID (0x1344 is assigned to Micron)
		13h	5		
	2	0000h	6–7	RO	Reserved
	2	Variable	8	RO	Temperature value (Celsius), little-endian
		Variable	9		

Table 24: Subsystem Management Data (SMD) Structure

Address	#Bytes	Value	Byte Offset	Description
0x6A (7-bit)	1	06h	0	**Length of Status:** Indicates number of additional bytes to read before encountering PEC.
	1	Variable	1	**Length of Status:** Indicates number of additional bytes to read before encountering PEC.
				SMBus Arbitration: Bit 7 is set to 1 after an SMBus block read is completed all the way to the stop bit without bus contention and cleared to 0 if an SMBus send byte FFh is received on this SMBus slave address.
				Drive Not Ready: Bit 6 is set to 1 when the subsystem is not capable of processing NVMe management commands, and the rest of the transmission may be invalid. If cleared to 0, then the NVM subsystem is fully powered and ready to respond to management commands. This logic level intentionally identifies and prioritizes powered up and ready drives over their powered off neighbors on the same SMBus segment.
				Drive Functional: Bit 5 is set to 1 to indicate an NVM subsystem is functional. If cleared to 0, then there is an unrecoverable failure in the NVM subsystem and the rest of the transmission may be invalid.
				Reset Not Required: Bit 4 is set to 1 to indicate the NVM subsystem does not need a reset to resume normal operation. If cleared to 0 then the NVM subsystem has experienced an error that prevents continued normal operation. A controller level reset is required to resume normal operation.
				Port 0 PCIe Link Active: Bit 3 is set to 1 to indicate the first port's PCIe link is up (i.e., the data link control and management state machine is in the DL_Active state). If cleared to 0, then the PCIe link is down.
				Port 1 PCIe Link Active: Bit 2 is cleared to 0, the second port's PCIe link is not present.
	1	Variable	2	**SMART Warnings:** This field shall contain the critical warning field (byte 0) of the NVMe SMART/Health Information log. Each bit in this field shall be inverted from the NVMe definition (i.e., the management interface shall indicate a 0 value while the corresponding bit is 1 in the log page). Refer to the NVMe specification for bit definitions. Cleared to 0 if the NVM subsystem indicates a critical warning for the corresponding bit. Set to 1 if the NVM subsystem does not indicate a critical warning for the corresponding bit.

Table 24: Subsystem Management Data (SMD) Structure (Continued)

Address	#Bytes	Value	Byte Offset	Description
0x6A (7-bit)	1	Variable	2	**Composite Temperature (CTemp):** This field indicates the current temperature in degrees Celsius. If a temperature value is reported, it should be the same temperature as the composite temperature from the SMART log of hottest controller in the NVM subsystem. The reported temperature range is vendor specific, and shall not exceed the range –60 to +127°C. The 8-bit format of the data is shown below. This field should not report a temperature that is older than 5 seconds. If recent data is not available, the management endpoint should indicate a value of 80h for this field. 00h-7Eh: Temperature is measured in degrees Celcius (0°C to 126°C). 7Fh: 127° or higher. 80h: No temperature data or temperature data is more than 5 seconds old. 81h: Temperature sensor failure. 82h-C3h: Reserved. C4: Temperature is -60°C or lower. C5-FFh: Temperature measured in degrees Celcius is represented in two's complement (–1°C to -59°C).
	1	Variable	4	**Percentage Drive Life Used (PDLU):** Contains a vendor specific estimate of the percentage of NVM subsystem NVM life used based on the actual usage and the manufacturer's prediction of NVM life. A value of 100 indicates that the estimated endurance of the NVM in the NVM subsystem has been consumed, but may not indicate an NVM subsystem failure. The value is allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value should be updated once per power-on hour and equal the percentage used value in the NVMe SMART health log page.
	2	–	5-6	Reserved.
	1	Variable	7	**PEC:** An 8-bit CRC calculated over the slave address, command code, second slave address and returned data. The algorithm is defined in the SMBus specification.
	1	16h	8	**Length of Identification:** Indicates number of additional bytes to read before encountering PEC.
	2	13h	9	**Vendor ID:** The 2-byte vendor ID, assigned by the PCI SIG. Note the MSB is transmitted first.
		44h	10	
	20	Variable	11-30	**Serial Number:** 20 characters that match the serial number in the NVMe identify controller command response. Note the first character is transmitted first.
	1	Variable	31	**PEC:** An 8-bit CRC calculated over the slave address, command code, second slave address and returned data. The algorithm is defined in the SMBus specification.

Interface Connectors

Figure 3: Interface Connections – Enterprise PCIe (SFF-8639)

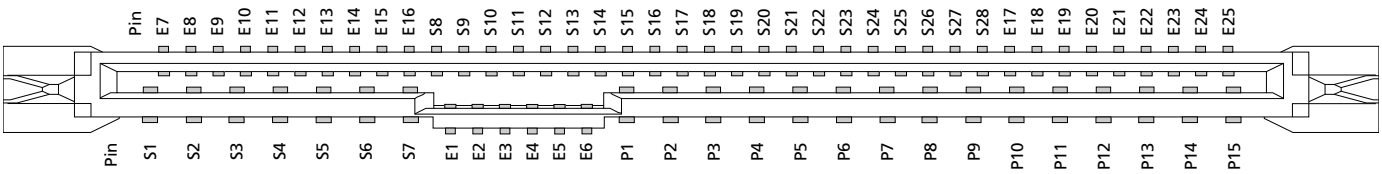


Table 25: Signal Assignments

Top Side			Bottom Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
S1	GND	No connect	E7	RefClk0+	PCIe REFCLK+
S2	S0T+ (A+)	No connect	E8	RefClk0-	PCIe REFCLK-
S3	S0T- (A-)	No connect	E9	GND	Ground
S4	GND	No connect	E10	PETp0	PCIe TX+ Lane 0
S5	S0R- (B-)	No connect	E11	PETn0	PCIe TX- Lane 0
S6	S0R+ (B+)	No connect	E12	GND	Ground
S7	GND	No connect	E13	PERn0	PCIe RX- Lane 0
E1	RefClk1+	No connect	E14	PERp0	PCIe RX+ Lane 0
E2	RefClk1-	No connect	E15	GND	Ground
E3	3.3Vaux	+3.3V	E16	RSVD	No connect
E4	ePERst1#	No connect	S8	GND	No connect
E5	ePERst0#	PERST#	S9	S1T+	No connect
E6	RSVD	No connect	S10	S1T-	No connect
P1	RSVD(Wake#)	No connect	S11	GND	No connect
P2	sPCIeRst	No connect	S12	S1R-	No connect
P3	RSVD(ClkReq#)	No connect	S13	S1R+	No connect
P4	IfDet#	Ground	S14	GND	No connect
P5	GND	Ground	S15	RSVD	No connect
P6	GND	Ground	S16	GND	Ground
P7	5V	No connect	S17	PETp1/S2T+	PCIe TX+ Lane 1
P8	5V	No connect	S18	PETn1/S2T-	PCIe TX- Lane 1
P9	5V	No connect	S19	GND	Ground
P10	PRSNT#	No connect	S20	PERn1/S2R-	PCIe RX- Lane 1
P11	Activity	Drive activity signal	S21	PERp1/S2R+	PCIe RX+ Lane 1
P12	GND	Ground	S22	GND	Ground
P13	12V	+12.0V	S23	PETp2/S3T+	PCIe TX+ Lane 2
P14	12V	+12.0V	S24	PETn2/S3T-	PCIe TX- Lane 2

Table 25: Signal Assignments (Continued)

Top Side			Bottom Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
P15	12V	+12.0V	S25	GND	Ground
–	–	–	S26	PERn2/S3R-	PCIe RX- Lane 2
–	–	–	S27	PERp2/S3R+	PCIe RX+ Lane 2
–	–	–	S28	GND	Ground
–	–	–	E17	PETp3	PCIe TX+ Lane 3
–	–	–	E18	PETn3	PCIe TX- Lane 3
–	–	–	E19	GND	Ground
–	–	–	E20	PERn3	PCIe RX- Lane 3
–	–	–	E21	PERp3	PCIe RX+ Lane 3
–	–	–	E22	GND	Ground
–	–	–	E23	SMClk	SMBus clock
–	–	–	E24	SMDat	SMBus data
–	–	–	E25	DualPortEn#	No connect

PCI Express Configuration Space Headers

Figure 4: 9300 PRO PCIe Configuration Space Header

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0	Byte offset
Device ID (DID) = 51B1h		Vendor ID (VID) = 1344h		00h
		Command register		04h
		Status register		06h
			Revision ID (RID) = 0x01	08h
	Base class code (BCC) = 0x01	Subclass code (SCC) = 0x08	Programming interface (PI) = 0x02	09h
			Cache line size (CLS)	0Ch
Memory address register base address lower (BAR0)				10h
Memory address register base address upper (BAR1)				14h
Index data pair register base (BAR2)				18h
Subsystem ID (SSID) = 4000h (3.84TB U.2) Subsystem ID (SSID) = 5000h (7.68TB U.2) Subsystem ID (SSID) = 6000h (15.36TB U.2)		Subsystem vendor ID (SSVID) = 1344h		2Ch

Figure 5: 9300 MAX PCIe Configuration Space Header

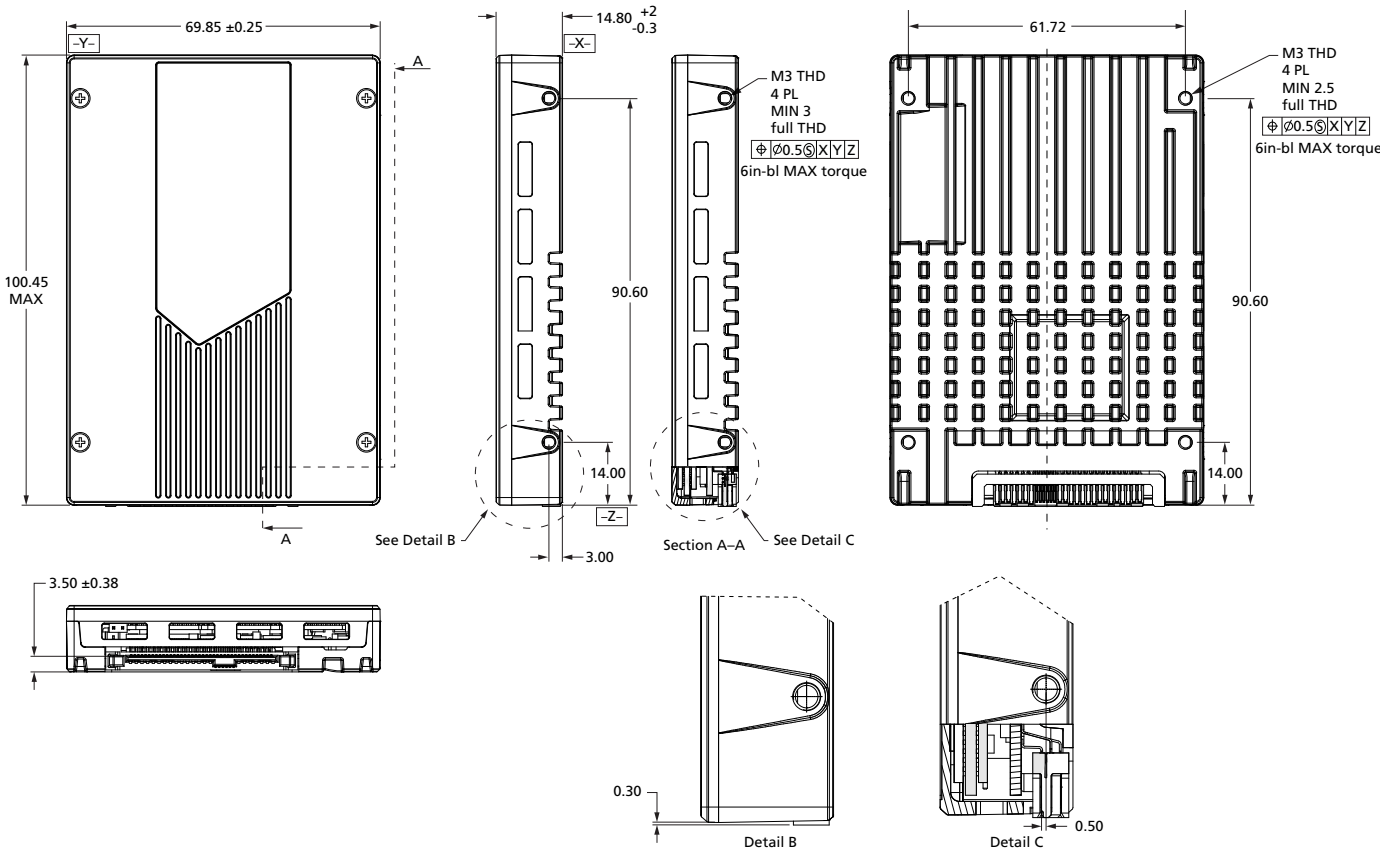
Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0	Byte offset
Device ID (DID) = 51B2h		Vendor ID (VID) = 1344h		00h
		Command register		04h
		Status register		06h
			Revision ID (RID) = 0x01	08h
	Base class code (BCC) = 0x01	Subclass code (SCC) = 0x08	Programming interface (PI) = 0x02	09h
			Cache line size (CLS)	0Ch
Memory address register base address lower (BAR0)				10h
Memory address register base address upper (BAR1)				14h
Index data pair register base (BAR2)				18h
Subsystem ID (SSID) = 4000h (3.2TB U.2) Subsystem ID (SSID) = 5000h (6.4TB U.2) Subsystem ID (SSID) = 6000h (12.8TB U.2)		Subsystem vendor ID (SSVID) = 1344h		2Ch

Physical Configuration

U.2 (2.5") 15mm

Product mass: less than 235 grams

Figure 6: U.2 (2.5") Nominal Dimensions



Notes:
1. All dimensions are in millimeters.
2. Length does not include 0.3 connector protrusion.

Table 26: U.2 (2.5") Maximum Dimensions

Capacity (TB)	Width	Length	Height	Unit
3.2	70.10	100.45	15.00	mm
3.84				
6.4				
7.68				
12.8				
15.36				

Compliance

Micron SSDs comply with the following:

- Micron Green Standard
- Built with sulfur-resistant resistors
- CE (Europe): EN55032, EN55024 Class B, RoHS
- FCC: CFR Title 47, Part 15, Class B
- UL/cUL: approval to UL-60950-1, 2nd Edition, IEC 60950-1:2005 (2nd Edition); EN 60950-1 (2006) + A11:2009+ A1:2010 + A12:2011 + A2:2013
- BSMI (Taiwan): approval to CNS 13438, Class B, CNS 15663
- RCM (Australia, New Zealand): AS/NZS CISPR32 Class B
- KC RRL (Korea): approval to KN32 Class B, KN 35 Class B

B 급 기기	이 기기는 가정용으로 전자파적합등록을한 기기로서 주거
(가정용 정보통신기기)	지역에서는 물론 모든지역에서 사용할 수 있습니다.

- W.E.E.E.: Compliance with EU WEEE directive 2012/19/EC. Additional obligations may apply to customers who place these products in the markets where WEEE is enforced.
- TUV (Germany): approval to IEC60950/EN60950
- V_{CCI} (Japan): 2015-04 Class B

この装置は、クラス B 情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
取扱説明書に従って正しい取り扱いをして下さい。
VCCIーB

- IC (Canada): ICES-003 Class B
  - This Class B digital apparatus complies with Canadian ICES-003.
  - Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.
- Morocco: EN55032, EN55024 Class B
- UkrSEPRO (Ukraine): EN55032 Class B, IEC60950/EN60950, RoHS (Resolution 2017 No. 139)

FCC Rules

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

References

- NVM Express, Revision 1.2
- PCI Express Base Specification, Revision 3.1
- PCI Express Card Electromechanical (CEM), Revision 3.0
- PCI Express SFF-8639 Module Specification, Revision 3.0, Version 1.0
- Enterprise SSD Form Factor Version 1.0a
- NVM Express Management Interface, Revision 1.0
- IDEMA Standard LBA 1-03
- Telcordia Reliability Prediction Procedure for Electronic Equipment SR-332

Revision History

Rev. A – 03/19

- Initial release

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www.micron.com/products/support Sales inquiries: 800-932-4992

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.